REMARKS

Favorable reconsideration and allowance of the present patent application are respectfully requested in view of the the following remarks. Claim 17-32 were pending prior to the Office Action. Claims 33-58 have been added by the Reply. Therefore, claims 17-58 are pending. Claims 17, 33, and 47 are independent.

Drawings

In the Office Action, the Drawings were objected to for informalities. More specifically, Figure 1 was objected for not including a legend. Figure 1 has been amended as suggested. Applicants request that the objection to Figure 1 be withdrawn.

32 U.S.C. § 102 Rejection Based on Zavracky

Claims 17-32 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Zavracky et al. (USPN 5,793,115) ("Zavracky"). Applicants respectfully traverse.

For a Section 102 rejection to be valid, the cited reference must teach or suggest each and every claimed element. *See M.P.E.P. 2131; M.P.E.P. 706.02.* Thus, if the cited reference fails to teach or suggest one or more elements, then the rejection must fail.

In this instance, Zavracky fails to teach or suggest each and every claimed element. For example, independent claim 17 recites, *inter alia*, "wherein the electrical conducting structures are formed by the electrical conducting portions in the sublayer ... are provided in registering connection with corresponding electrical conducting portions in one or more adjacent sublayers, such that the electrical conducting structures integrated in the sublayers form three-dimensional electrical interconnecting networks in the layers." Zavracky fails to teach or suggest at least this feature.

More specifically, Zavracky is directed toward forming three-dimensional processor using transferred thin film circuits. Zavracky discloses that interlayer connections 140 are used to electrically connect multiple layers. *See Figure 1; column 6, lines 43-45.* It is noted that the interlayer connections 40 are formed by etching holes 414, 416 where connections are desired and then laying down a metallization layer 422 to connect the exposed metal pad 420 of the second layer to the exposed metal pad 418 of the first layer. *See Figure 4; column 8, lines 29-33.* Thus, at best, the metallization layers 422 may be said to form three-dimensional electrical interconnecting networks.

However, it is noted that the metallization layer 422 is a single unit that spans multiple layers. In other words, there is no disclosure that portions of the metallization layer 422 are formed in a sublayer by sublayer manner to form registering connections. Thus, Zavracky does not teach or suggest

electrical conducting structures formed by the electrical conducting portions in the sublayer in registering connection with corresponding electrical conducting portions in one or more adjacent sublayers, such that the electrical conducting structures integrated in the sublayers form three-dimensional electrical interconnecting networks in the layers. Therefore, for at least this reason, independent claim 17 is distinguishable over Zavracky.

Claims 18-32 depend from claim 17, directly or independently. Therefore, for at least the reasons stated with respect to claim 17, claims 18-32 are also distinguishable from Zavracky.

Applicant respectfully requests that the rejection of claims 17-32, based on Zavracky, be withdrawn.

NEW CLAIMS

Claims 33-58 have been added through this reply. All new claims are believed to be distinguishable over the cited references, individually or in any combination. For example, claim 58 depends from independent claim 17. Therefore, claim 58 is allowable over the cited reference for at least the reasons stated with respect to claim 17.

Also, independent claim 33 recites, *inter alia*, "wherein at least one main layer includes logic devices formed from organic materials." Independent claim 47 also recites a similar feature. It is noted that in Zavracky, all the layers discloses are silicon based semiconductor technology. For example, the first

layer 200 is built upon silicon substrate upon which microprocessor logic blocks are fabricated. *See column 5, lines 37-40.* The second layer 100 is formed from a thin film of silicon material and uses silicon-on-insulator techniques. *See Figures 3A-3H; column 7, lines 10-50.* Zavracky fails to teach or suggest using organic materials of any kind. Thus independent claims 33 and 47 are also allowable.

Claims 34-46 and 48-58 depend from independent claims 33 and 47, directly or indirectly. Thus, for at least the reasons stated with respect to the independent claims, these dependent claims are also allowable.

In addition, dependent claim 35 recites, *inter alia*, "vertically conducting structure is from aligned corresponding vertically conducting portions of at least two adjacent sublayers." Claim 49 recites a similar feature. It has been shown above that Zavracky does not teach or suggest at least this feature.

For at least the reasons stated above, new claims 33-58 are distinguishable over the cited reference. Applicants respectfully request that the new claims be allowed.

CONCLUSION

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Hyung Sohn (Reg. No. 51,423), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2525 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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